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A REFRACTORY SELF-ALIGNED GATE PROCESS FOR MONOLITHICALLY COMBINED MICROWAVE AND DIGITAL GaAs ICs

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Abstract

We present a process for monolithically fabricating microwave and DCFL digital GaAs circuits. The process employs refractory metal SAG FETs with techniques to provide low gate resistance and high output resistance and breakdown voltage. Using a 1.0 μm gate length, 1.5 dB noise figure with 10.2 dB associated gain at 10 GHz analog performance and 65 ps typical propagation delay at 0.5 mW/gate (fan-in/fan-out = 2/2) DCFL digital performance have been obtained.

Introduction

We present a process for monolithically fabricating combined microwave and digital GaAs integrated circuits. The process is based on a refractory metal self-aligned gate FET, which employs an n+ implant that is asymmetric with respect to the gate. This improves the microwave performance of the SAG FETs, especially power FETs. ITT is currently developing a limiting amplifier and counter subsystem that requires integrated analog and digital circuits, and the results will be presented at the conference.

The current combined analog and digital self-aligned gate (SAG) process is the result of an intense effort to unify GaAs IC fabrication at ITT. There were several reasons to establish a combined process. The first was to simplify the logistics of running our manufacturing line. ITT has run a standard recessed-gate MMIC line for small-signal and power IC's for the past four years and in addition, a refractory gate SAG digital process for the past two years. These processes differ significantly in process flow. A unified process offers enormous simplification in the logistics of running the line. Second, SAG processing has resulted in a dramatic improvement in uniformity and yield as compared to recessed gate processing of GaAs ICs manufactured at ITT. This is directly attributed to the removal of the highly operator-dependent and inherently non-uniform wet chemical gate recess etch. Third, while our recessed-gate process gives results comparable to the performance published in the literature for analog and digital circuits, we obtained such outstanding digital device and circuit results and microwave FET device results with the SAG process that we are expecting to obtain improved analog IC performance with the same process. Finally, the process unification based on a SAG FET technology allows for the incorporation of both analog and digital circuits on the same chip, using a relatively simple process with a minimum of mask levels.

Combined Analog and Digital SAG Process

The circuit fabrication process is very similar to the ITT refractory metal self-aligned gate (SAG) digital process described previously [1], except for the details of the FET channel and the addition of a second level of global metal using a plating process. The process is as follows. Two-inch LEC substrates are passivated with 85 nm of PECVD silicon oxynitride (SiON), through which selective implants of ^{29}Si are performed for enhancement- and depletion-mode digital FETs, small-signal and power analog FETs and resistors. The passivation layer is then removed and a 200 nm film of TiWN is reactively sputtered onto the wafers.

The TiWN layer is patterned into "T-gate" structures (see Fig 1a) by liftoff of a Ni etch mask and subsequent reactive ion etching in CF_4/O_2 plasma. The digital FETs then receive a standard self-aligned n+ implant, during which the T-gate acts as the self-aligned n+ mask. The analog FETs receive the same n+ implant, but

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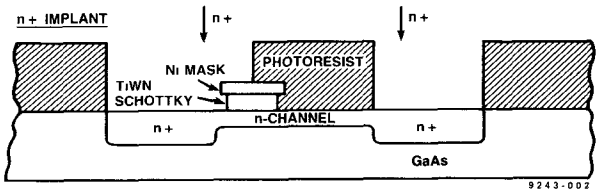
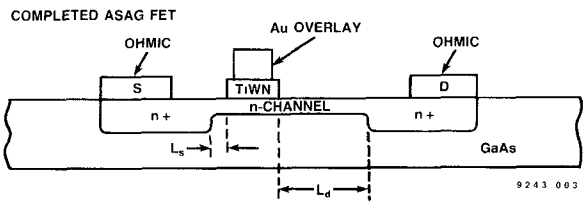
they have an additional masking of the n+ implant on the drain side of the gate via a stripe of photoresist (Fig 1a). After removal of the resist and Ni, the wafer is capped with 200 nm of SiON and annealed at 810°C for 20 min to activate the implants. Ohmic contacts are then formed by liftoff and alloying of AuGe/Ni (Fig 1b).



(1a) Schematic of "T-gate" structure with photoresist stripe on drain side of gate, which forms the n+ implantation mask.



(1b) ASAG FET with ohmic and gate metals in place.

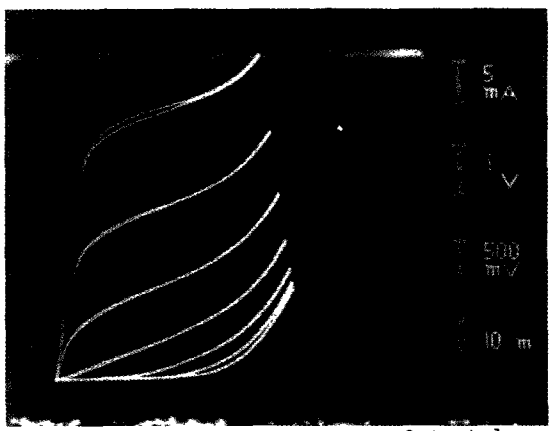
Note that L_s is equal to the Ni overhang ($\simeq$ 0.1 µm) resulting in very low R_s, while L_d is much larger ($\simeq$ 1 µm).

Fig. 1 Asymmetric Self-Aligned Gate (ASAG) FET.

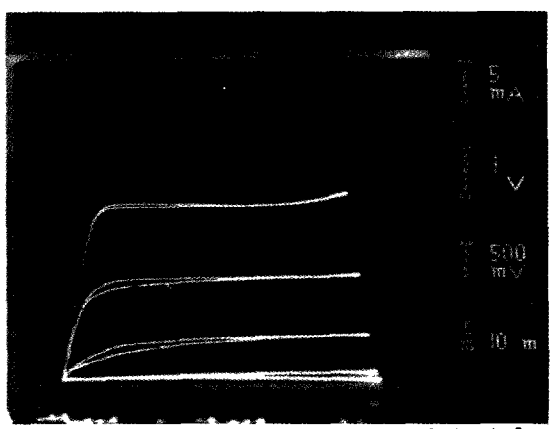
The circuits are then completed by defining two and one-half levels of interconnect metallization. The first half-level (600 nm TiPdAu) is defined by liftoff and forms the bottom plate of the microwave capacitors. It is also used to reduce the gate resistance of the FETs; a 0.5 µm long finger of metal is overlayed on the 1.0 µm long Schottky contact (see Fig 1b). The realignment tolerance of 0.25 µm is readily accomplished in ITT's pilot line production environment. Next 200 nm of PECVD silicon nitride is deposited. This film functions as both an interconnect level separation and the microwave capacitor dielectric. The first global interconnect metal (600 nm TiPdAu) is then defined by liftoff. Finally, a second global interconnect metal is defined by gold plating.

Results and Discussion

The use of an asymmetric, self-aligned n+ implant results in a dramatic increase in the source-to-drain breakdown voltage and output resistance. A comparison between the drain characteristics of two devices, SAG and ASAG FETs fabricated on the same wafer, reveals that while the SAG FET shows source-to-drain breakdown at 4 V, the ASAG FET breakdown voltage is in excess of 10 V (see Fig 2). Also, relative to the SAG FET the ASAG FET exhibits much improved drain current saturation characteristics and higher output resistance. We attribute both of these improvements over a SAG FET to the increased separation between the drain n+ region and the drain edge of the gate afforded by the ASAG ASAG structure.



(2a) SAG FET Implantation Schedule 3.8E12 cm^{-2}, 90 keV $V_{bd} \simeq 3.5$ V



(2b) ASAG FET Implantation Schedule 5.3E12 cm^{-2}, 90 keV $V_{bd} > 10$ V

Fig. 2 IV-Characteristics of SAG vs. ASAG FETs (Lg = 1 µm, Wg = 150 µm). Note the excellent saturation characteristics of the ASAG vs. the SAG FET, indicating a higher output resistance for the ASAG FET.

The device parameters and measured performance of small-signal ASAG FETs with four 75 μm fingers (300 μm total periphery) and 1.0 μm gate length are summarized in Table I.

Table I: ASAG FET small-signal parameters (L_g = 1 μm, W_g = 300 μm)

g_m at I_{ds} = 10 mA	150 mS/mm
Gate-source capacitance	1.3 pF/mm
Gate breakdown voltage	> 10 V
Source-to-drain breakdown voltage at I_{dss}	> 10 V
Source resistance	2.2 Ω
Gate resistance	2.0 Ω
10 GHz Performance	
Noise Figure (NF)	1.5 dB
Assoc. Gate (G_{as})	10.2 dB

In addition, we have observed that the NF and G_{as} of ASAG FETs are very stable as a function of I_{ds}. Also the variations in FET parameters (e.g. g_m and R_o) vs. temperatures up to 100°C are significantly less than those of equal gate length recessed gate FETs. This greatly facilitates MMIC oscillator design over the military spec temperature range.

We also obtained preliminary results on the use of ASAG FETs as microwave power FETs and the results are very encouraging. Gain, output power, an d power-added efficiency at the 1dB compression point for a channel implant of 4.5E12 cm^{-2} at 150 keV are summarized in Table II.

Table II
ASAG FET Power Performance

Frequency	5.5 GHz	10 GHz
G_{1dB}	13 dB	9 dB
P_{1dB}	450 mW/mm	400 mW/mm
η_{ADD}	33%	28%

V_{ds} = 8 V, I_{ds} = 0.5 I_{dss}

It should be noted that SAG FETs could not function as power FETs due to their very low (< 2 V) source-drain breakdown voltage at the required higher-energy channel implant.

While asymmetric self-aligned n+ implantation yields dramatically improved analog performance, standard "T-gate" SAG processing is required for enhancement-mode digital FETs. Enhancement-mode SAG FETs for digital circuits have a threshold voltage of + 0.1 V and an average transconductance of 240 mS/mm, with standard deviations over a wafer typically about 3% for transconductance and 5% for threshold voltage. Typical DCFL gate propagation delay is 65 ps at 0.5 mW/gate power dissipation, with fan-in = fan-out = 2 (1). Divide-by-two circuits using a D-type flip flop have operated at 4.5 GHz with only 1.5 mW power consumption, giving a record 0.3 pJ figure of merit, while 8-bit shift registers consume only 58 mW of power and operate at 1.6 GHz.

Finally, we report preliminary reliability data for these FETs. As of this writing, seven refractory-gate ASAG FETs have undergone high temperature storage stress at 280°C for 400 hours. On average, I_{dss} has been reduced by 6% and g_m has been reduced by 2%.

Summary

A refractory self-aligned gate process for combined microwave and digital GaAs IC fabrication has been described. This process is based on a digital refractory SAG process. It incorporates techniques to provide low gate resistance and high breakdown voltage and output resistance in order to improve the microwave performance of SAG FETs. Using this process, we have obtained small signal FETs with NF = 1.5 dB and G_{as} = 10.2 dB at 10 GHz; power performance of 13 dB gain, 450 mW/mm output power and 33% efficiency at the 1 dB compression point at 5.5 GHz; and enhancement-mode digital FETs with an average transconductance of 240 mS/mm. All of the above FET results have been achieved for a nominal 1 μm gate length FET simply by varying the ion-implantation schedules. The combined analog and digital process is currently being used by ITT to develop a limiting amplifier and counter subsystem which required analog and digital circuit functions. The results will be presented at the conference.

References

[1] H.P. Singh, R.A. Sadler, A.E. Geissberger, D.G. Fisher, J.A. Irvine, and G.E. Gorder, "A Comparative Study of GaAs Logic Families Using Universal Shift Registers and Self-Aligned Gate Technology," 1986 GaAs IC Symp. Tech. Digest, pp. 11-14 (1986).